

Implementation of a Multi Channel Modem for DSRC system on a Signal Processing Platform for Software Defined Radio

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- 1. Introduction**
- 2. Our Proposed “Reconfigurable Packet Routing oriented Signal Processing Platform” (RPPP)**
- 3. Implementation of DSRC Modem on RPPP**
- 4. Evaluation of logic usage efficiency**
- 5. Performance Evaluation (by HDL Simulator)**
- 6. Conclusion**

- In order to deploy various wireless and broadcasting media in vehicles, **Software Defined Radio(SDR) Technology** stands out as a promising approach.
- In a vehicle, **a number of wireless media are used simultaneously**.
To handle different radio systems, function of SDR is to be changed adaptively.
- We proposed
**“a reconfigurable packet routing-oriented signal processing platform”
(RPPP)**
to dynamically adapt FPGA based SDR system
for variety of radio signal processing in a vehicle.

- Intelligent Transport Systems (ITS) will use diversified communications technologies
- In Japan the ETC(Electric Toll Collection) vehicle unit is rapidly catching market: the number of devices installed has grown to **over 6 million** with a more than **41% utilization** rate on expressways.

→ for future functions based on DSRC system will be needed and deployed for many applications for vehicles

Therefore in-vehicle-unit need to handle **multi DSRC system communications** with efficient logic utilization on signal processing.

1-2. Aim of This Development

- build **multi-channel** Modem for DSRC system
with **diminishing the total logic scale**
based on our proposed signal processing platform for SDR
- **evaluate “the logic usage efficiency and the performance”**
of this multi-channel Modem

2. Our Proposed Platform “RPPP”

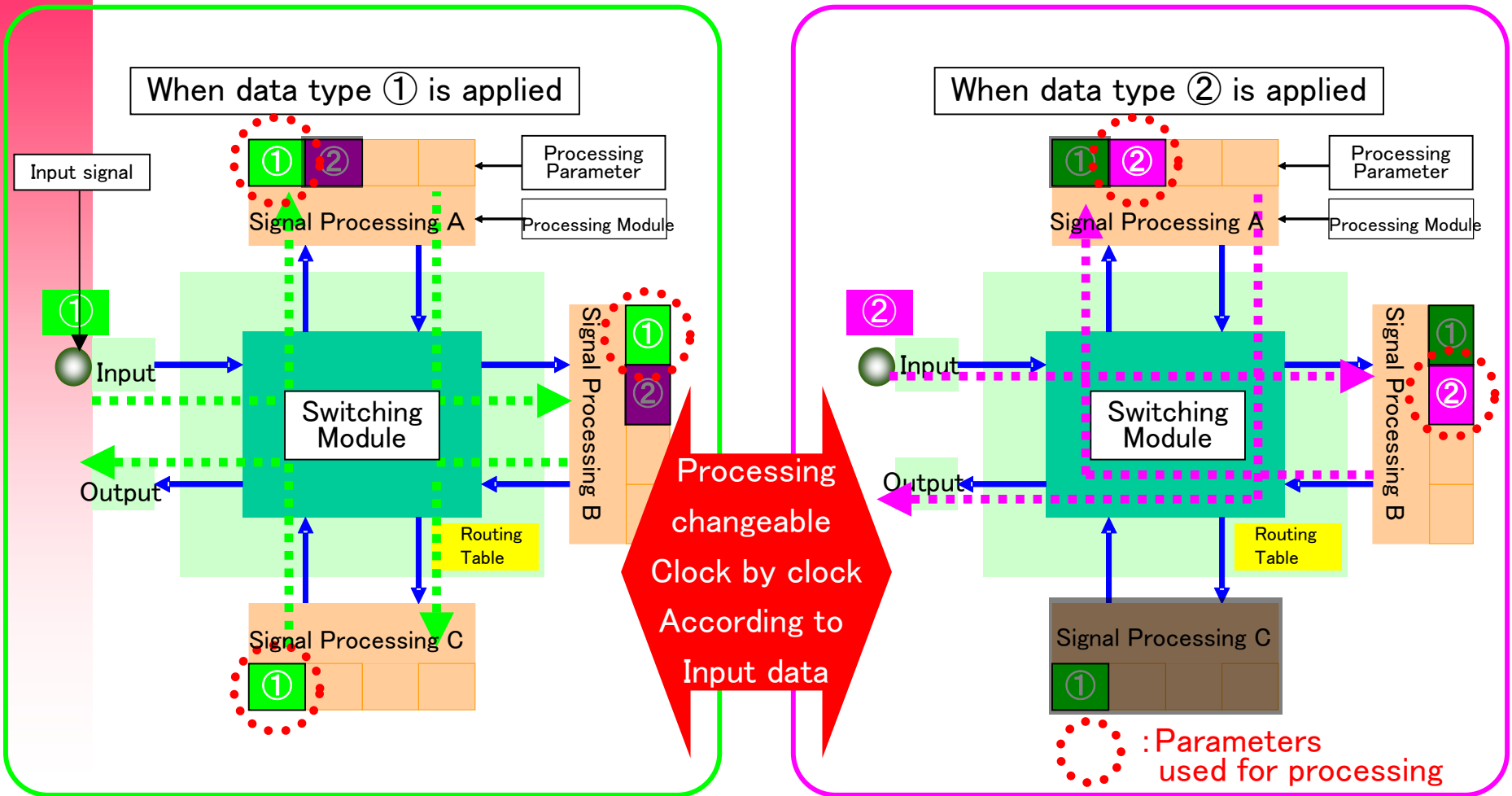
Reconfigurable Packet Routing-oriented Signal Processing Platform

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- (1) Composed of **Processing module** and **Switching module**
- (2) Signal data are packetized into **fixed 32bit length data packet**
- (3) Signal Processing are executed to the data packet by
Routing Processing by Switching Module
Sub Signal Processing by Processing Module

2-1. Structure of RPPP



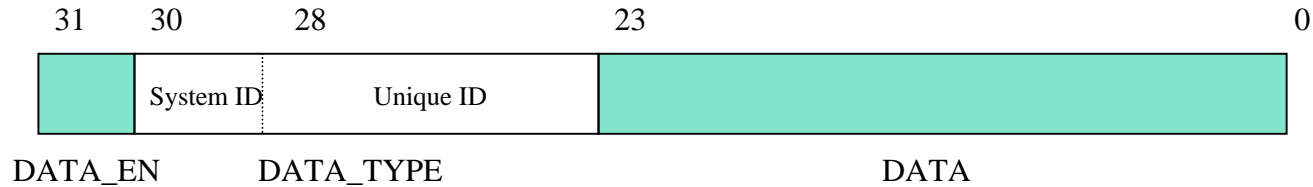
Features

- signal processing is subdivided to common “Processing Modules”, and each of them are connected with “Switching Modules” which execute routing to data packet.

2-2. Feature of RPPP

- (1) **High Logic usage efficiency** for each processing module by commonize processing logic with max. 4 type.
- (2) **High processing performance** by Distributed Parallel processing
- (3) **Fast switching ability** of signal processing - clock by clock
- (4) **High scalability** by adding each module

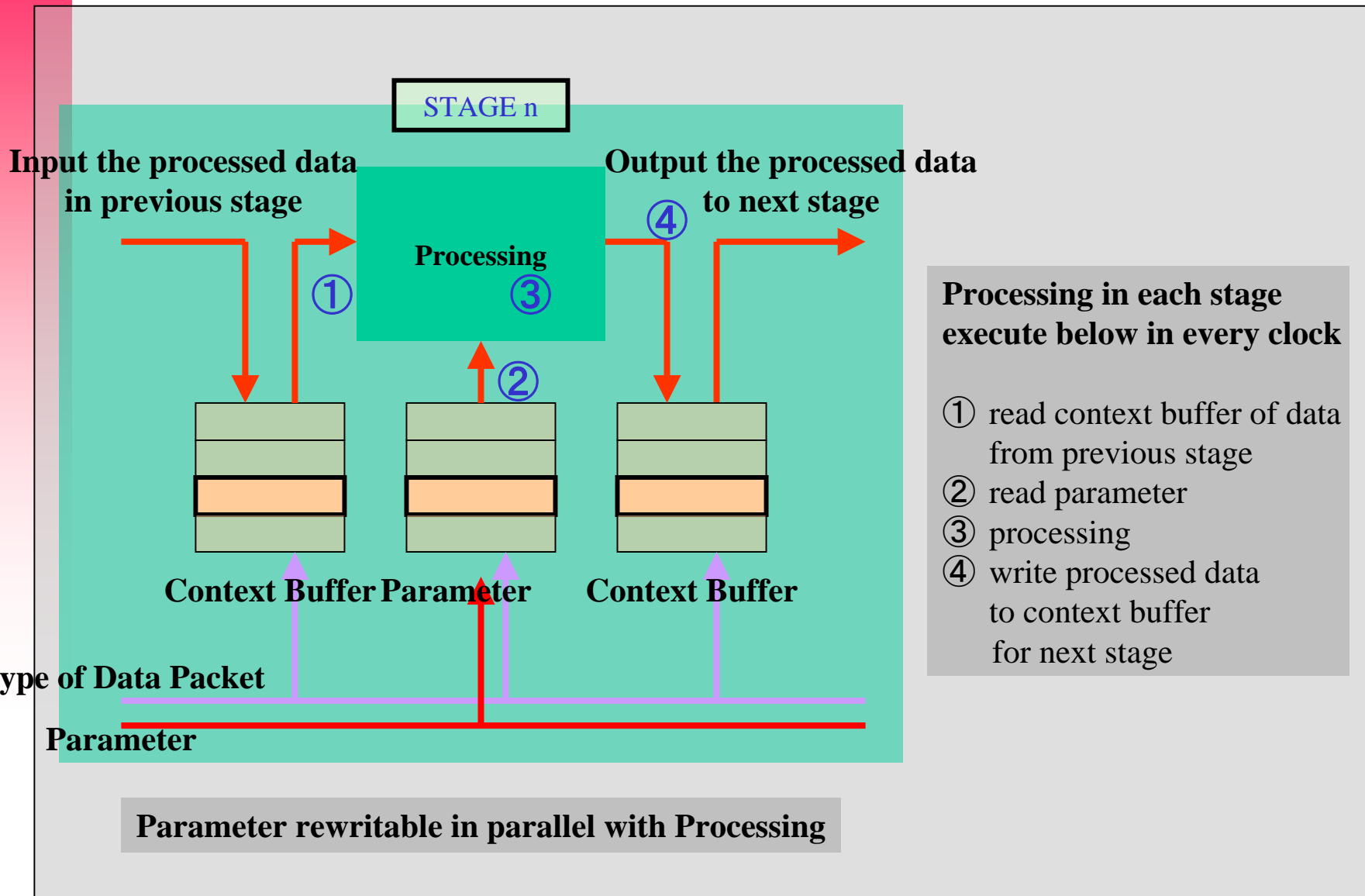
2-3. Format of Data Packet



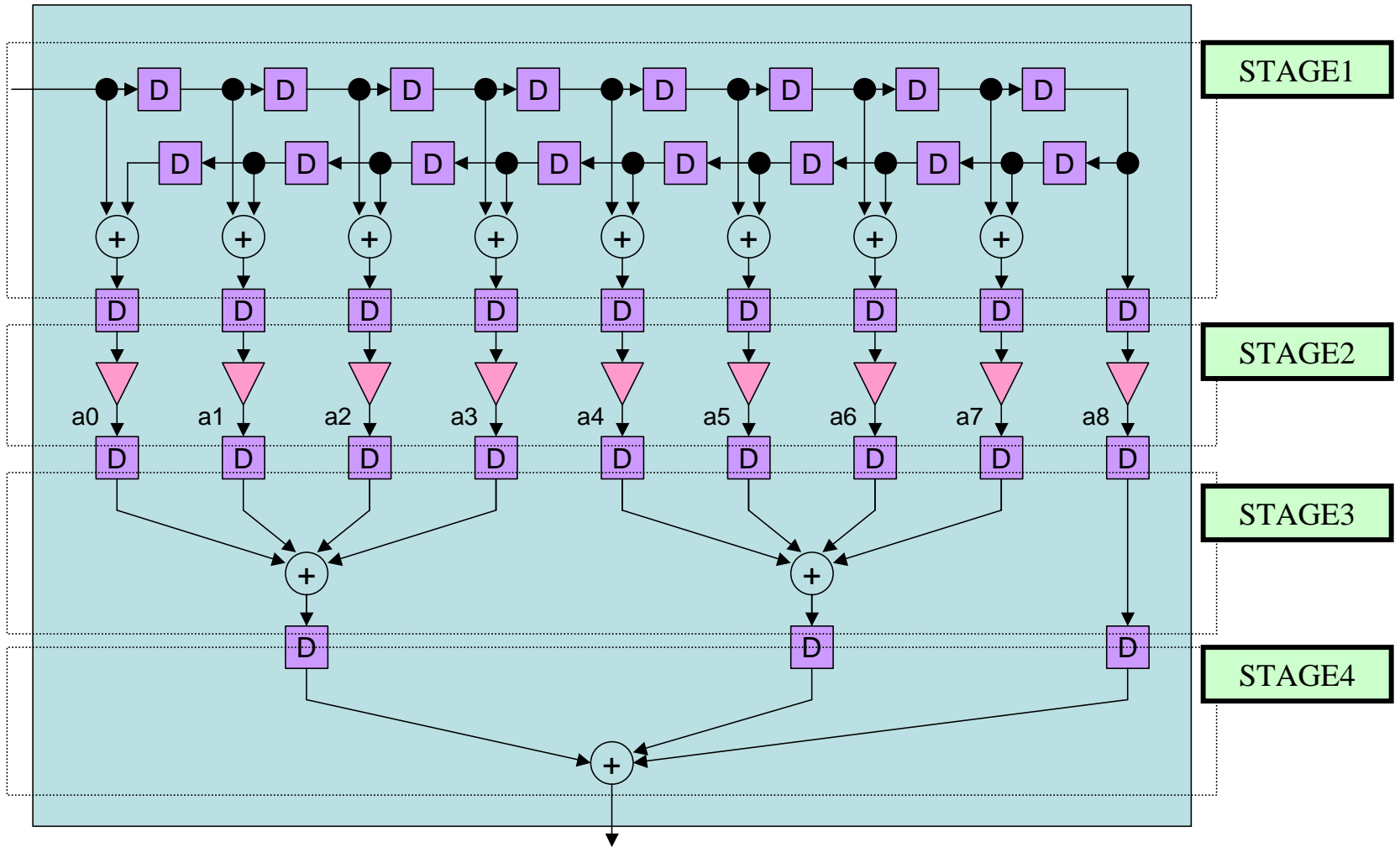
name	bit width	content
DATA	24	Signal Payload
DATA_TYPE	7	Data Type [6 downto 5] : System ID [4 downto 0] : Unique ID
DATA_EN	1	Data Validity

• **DATA_TYPE** show the system of its belongings and progress

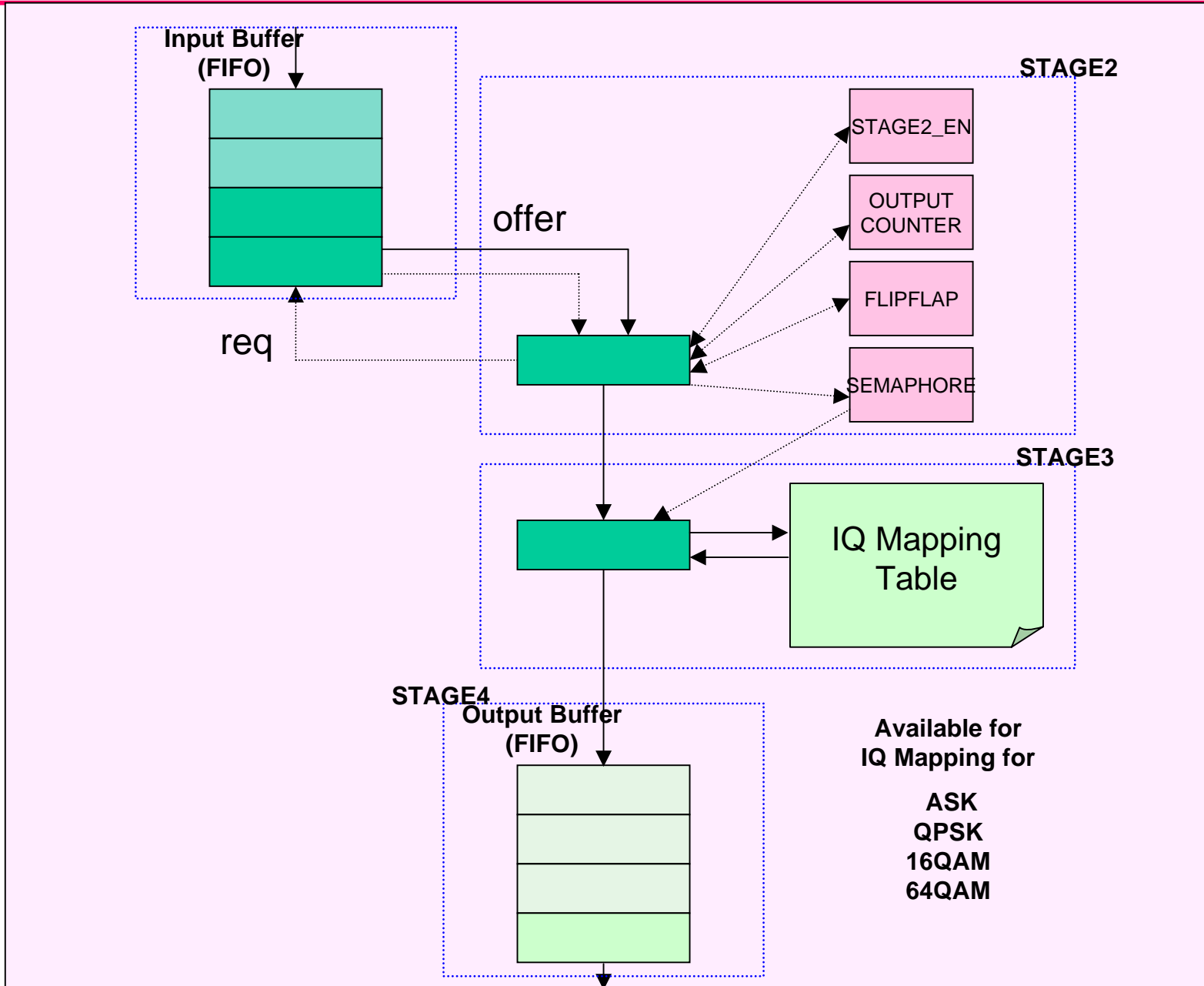
2-5. Structure of Processing Module



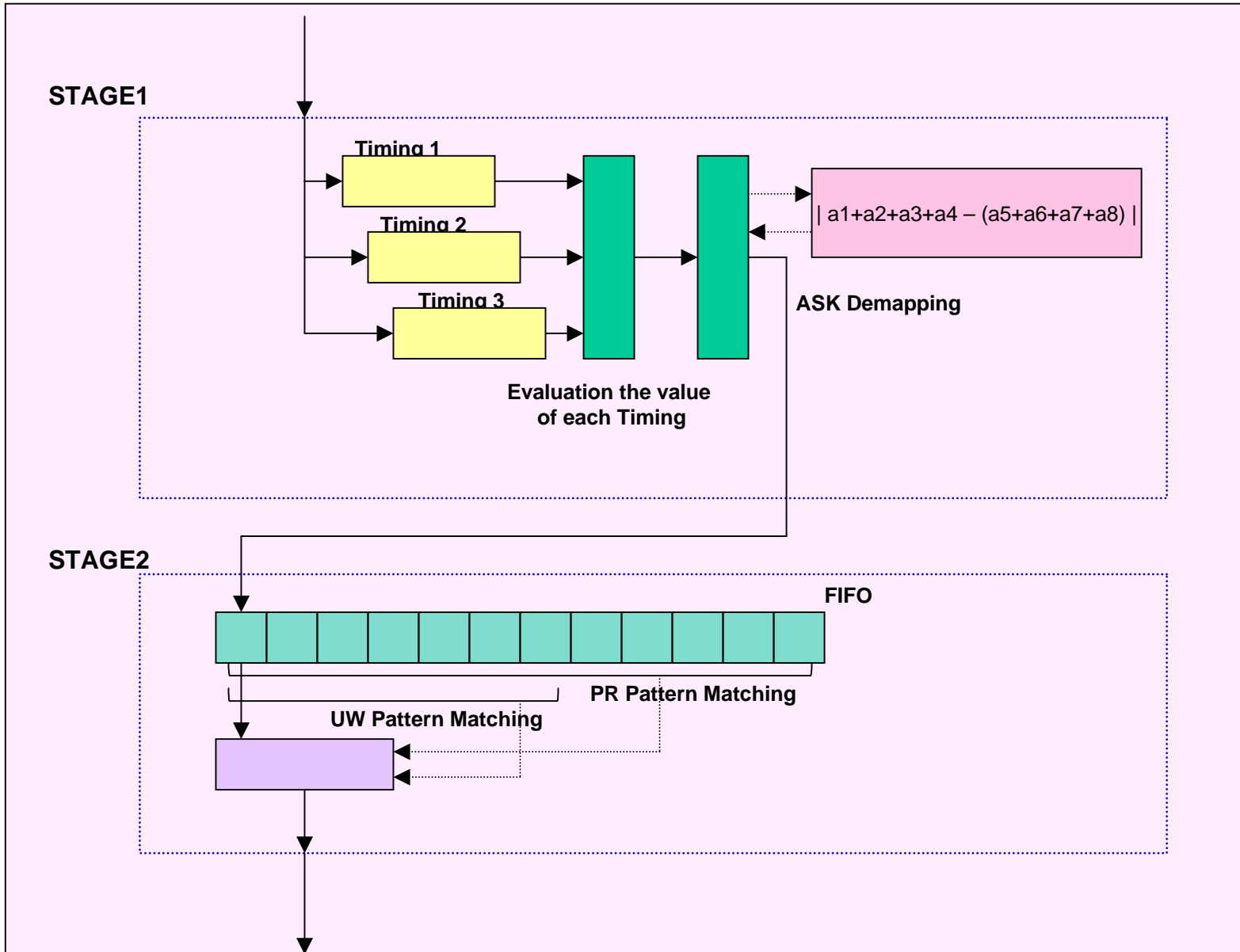
2-6-1. FIR Filtering Module



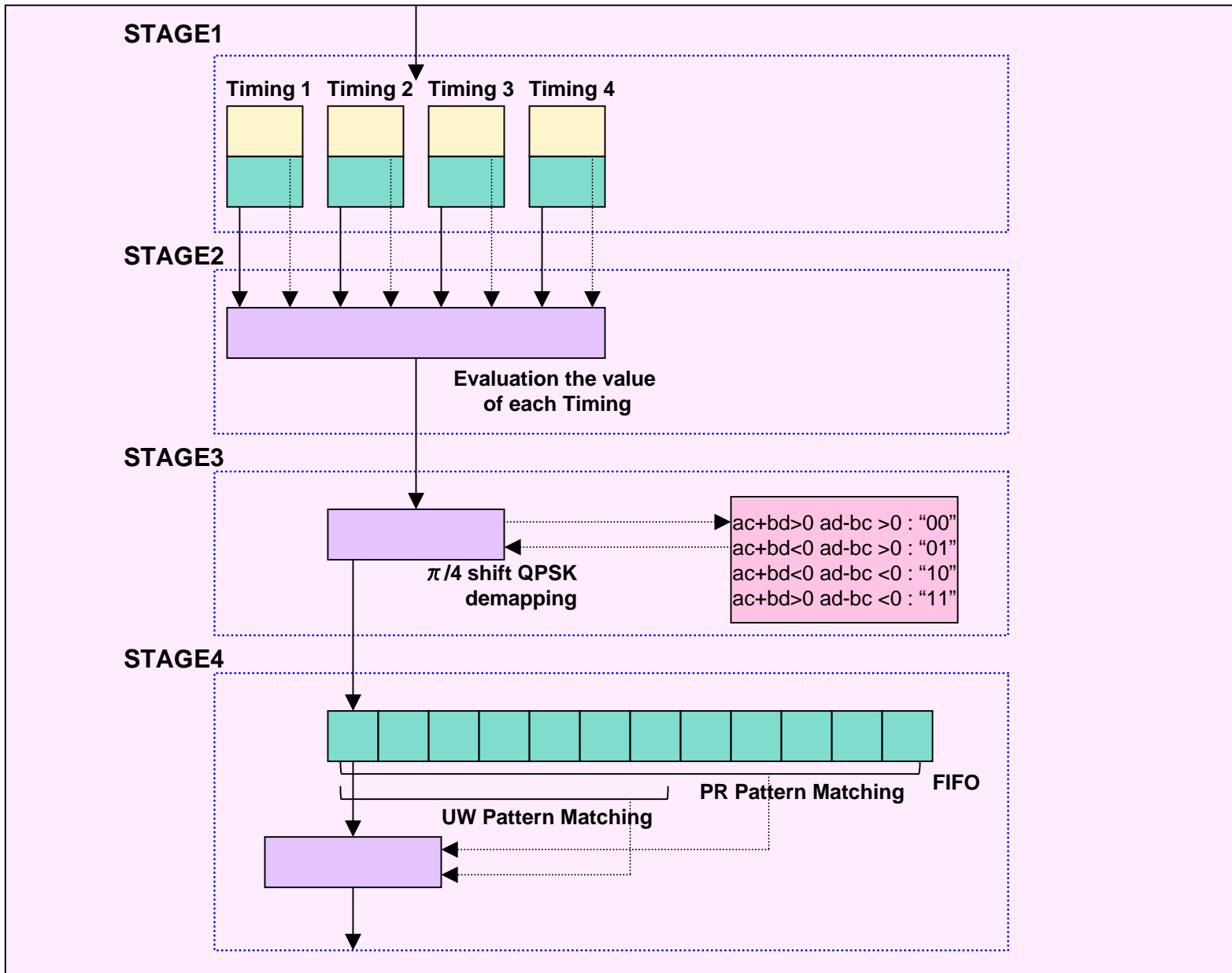
2-6-2. Mapper Module



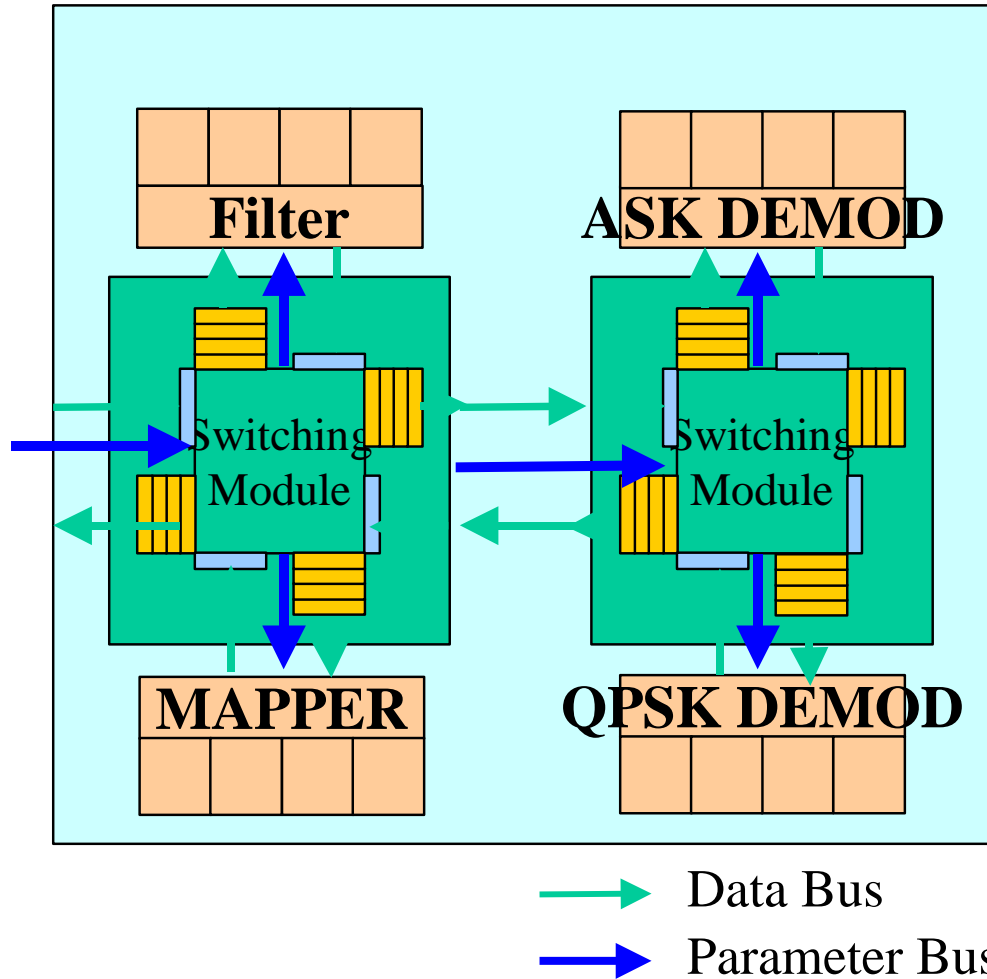
2-6-3. ASK Demodulation Module



2-6-4. $\pi/4$ shift QPSK Demodulation Module



3. Platform for Multi-Channel DSRC Modem

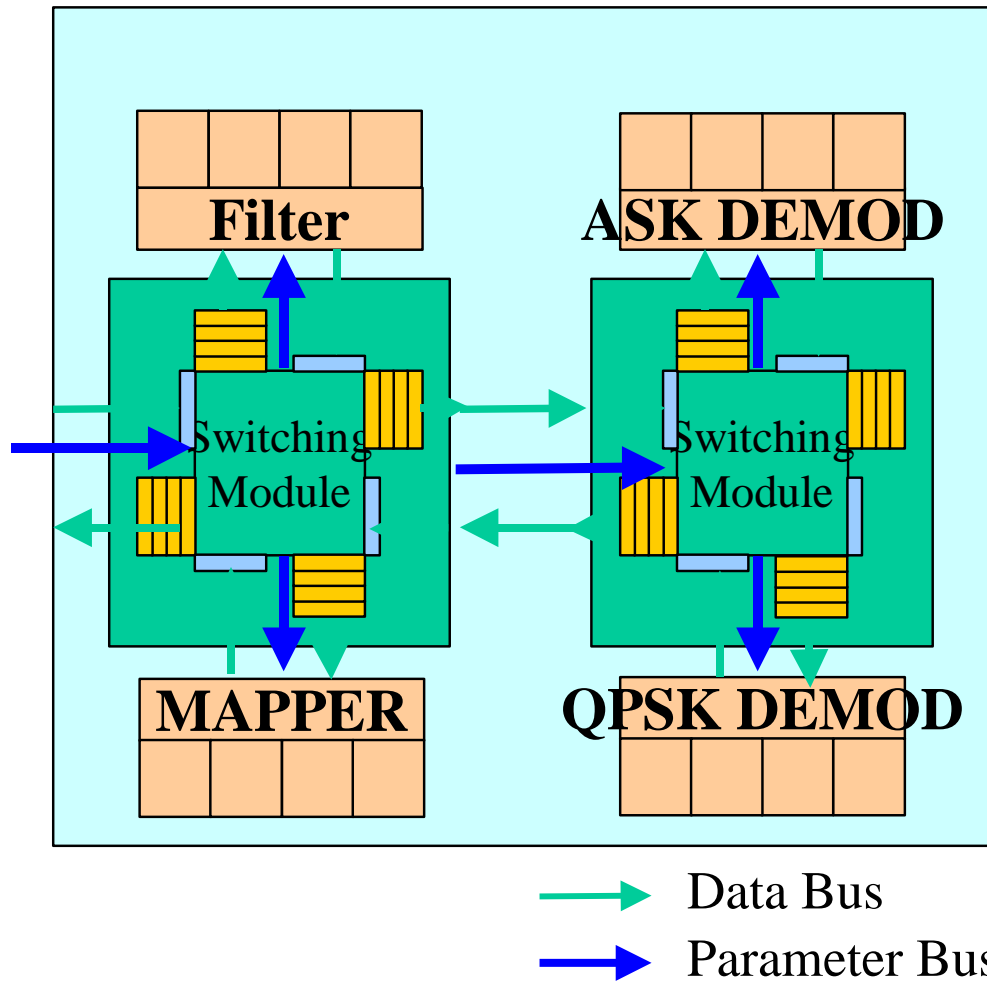


• Composed of 2 switching modules and 4 processing modules

modulation : MAPPER + Filter

demodulation : demodulator for each modulation

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4-2. Logic Usage Evaluation ~Total System~

※with Xilinx ISE 6.3.03i

modules with fixed parameter (conventional design)

	logic num (slices)	multiplier	subtotal logic num (slices)
FILTER	2396	4	9584
MAPPER	499	2	998
ASK_DEMOD	517	4	2068
QPSK_DEMOD	948	4	3792
TOTAL			16442

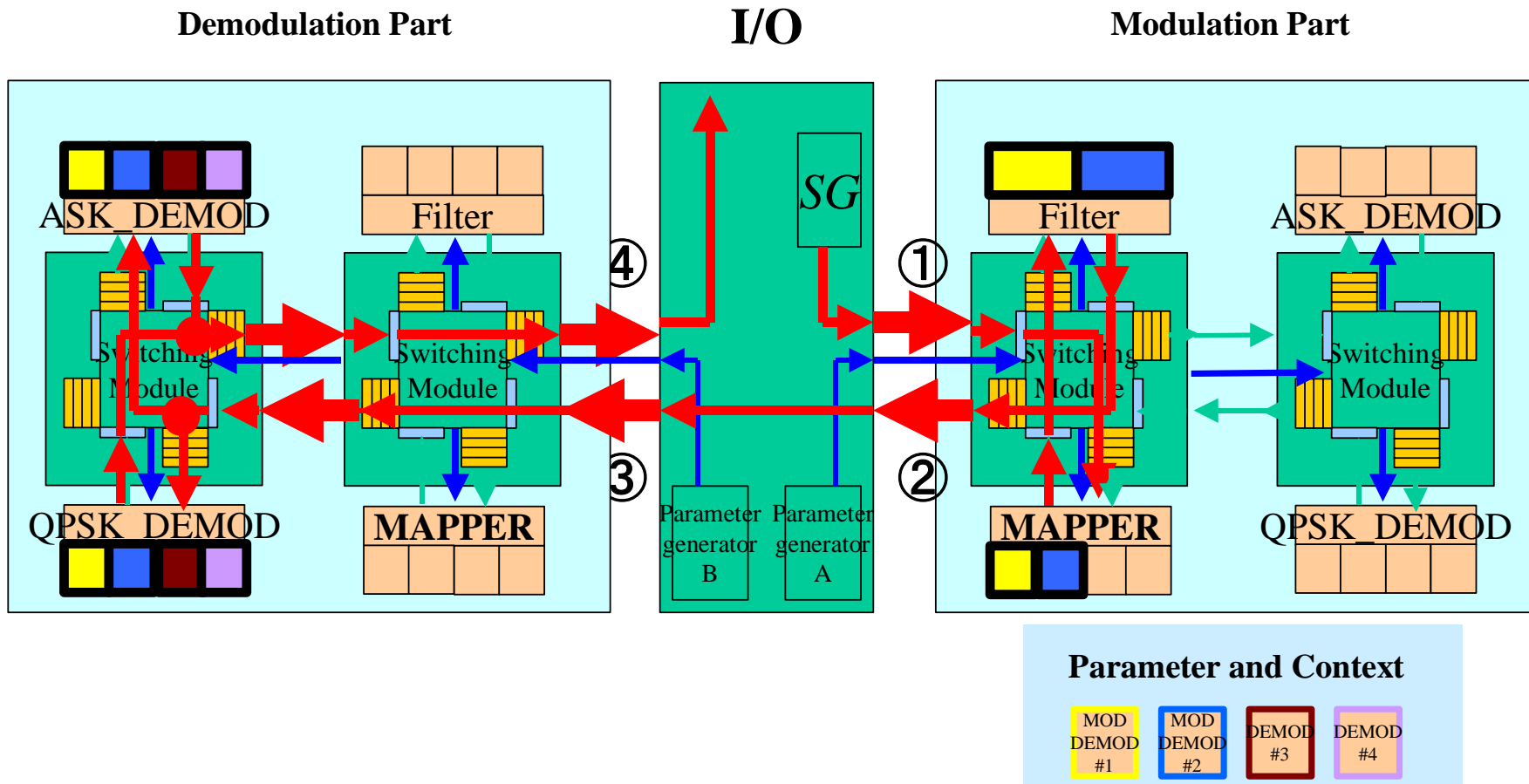
modules with controllable parameter (RPPP)

	logic num (slices)	multiplier	subtotal logic num (slices)
FILTER(4)	6885	1	6885
MAPPER(2)	1091	1	1091
ASK_DEMOD(4)	836	1	836
QPSK_DEMOD(4)	2462	1	2462
SwitchingModule	925	2	1850
TOTAL			13124

20.18%
improved

• total logic usage is 20.18% smaller than that of conventional design

5. Simulation Model for Modem



- 2 MODEM are connected by way of I/O block
- each part of this model has ability to execute both modulation and demodulation

5-1. Simulation Results ~Single-channel Modulation~

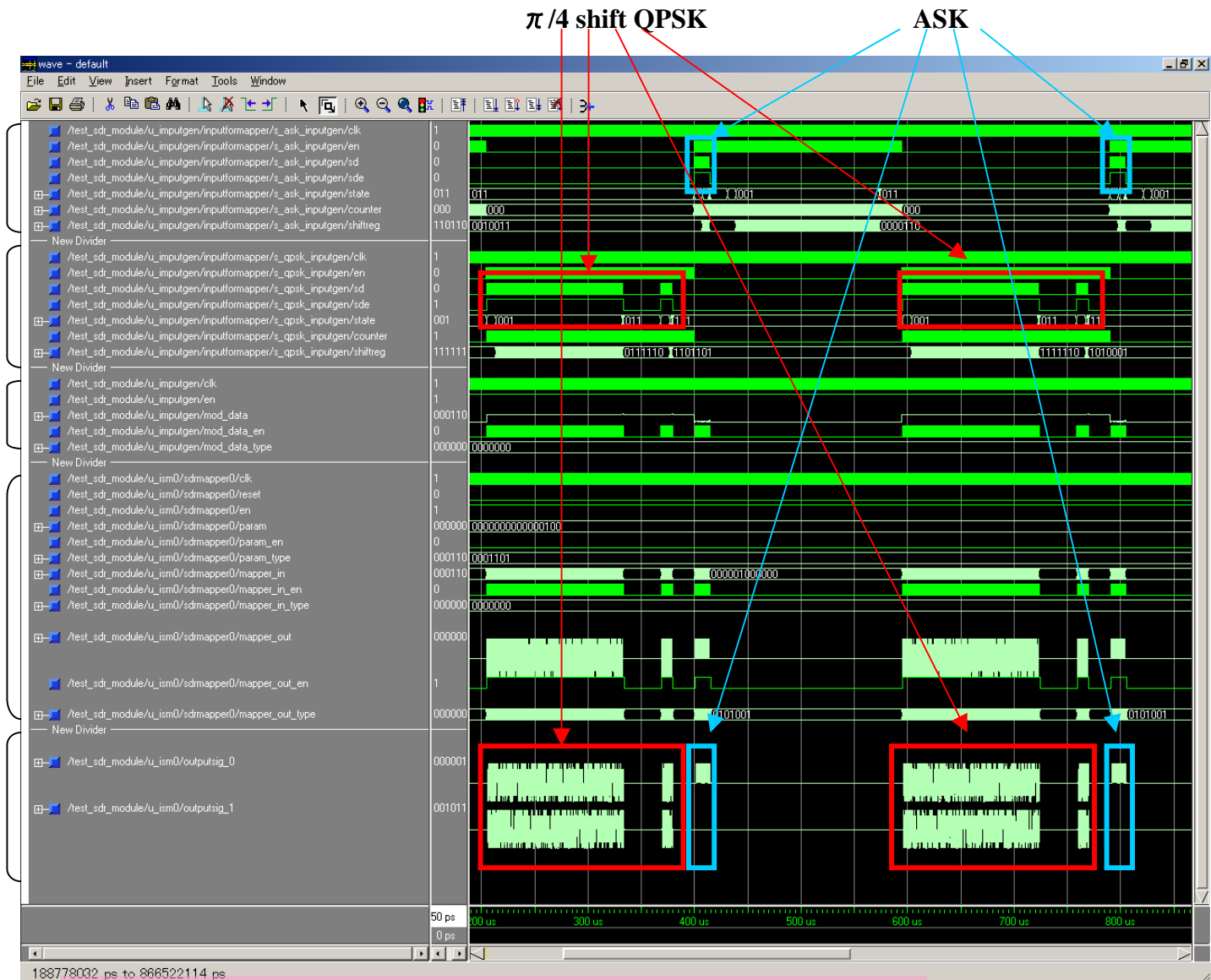
Input Signal
for ASK modulation

Input Signal
for $\pi/4$ shift QPSK

Input Signal to the
signal platform

signals in
Mapper Module

IQ signal
(after band-limit filter)



IQ modulation signals of ASK or $\pi/4$ shift QPSK are generated by Mapping and Nyquist Filtering.

5-2. Simulation Results ~Single-channel Demodulation~

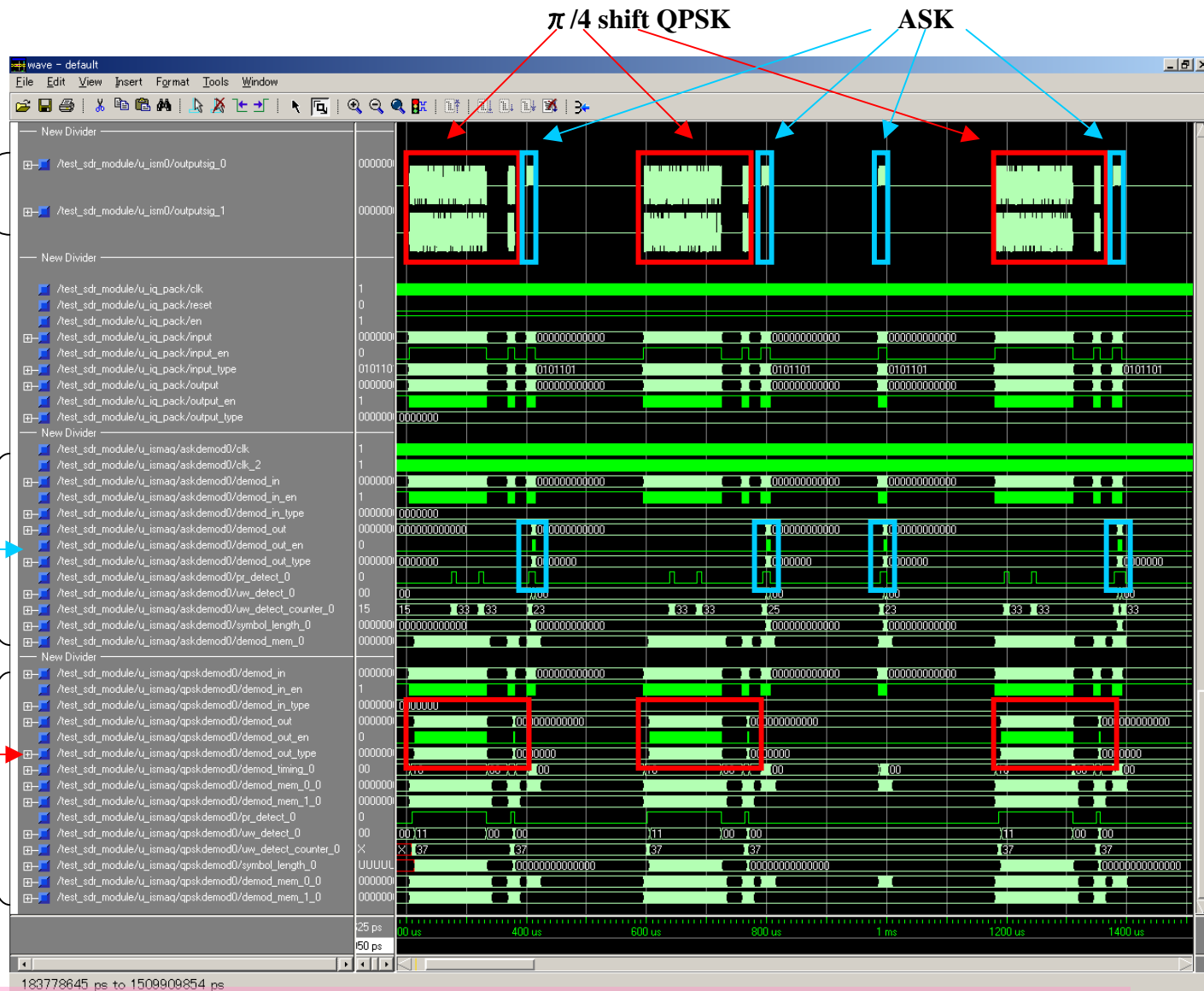
Input IQ signal for demodulation part

ASK demodulation module

demodulation output

$\pi/4$ shift QPSK demodulation module

demodulation output



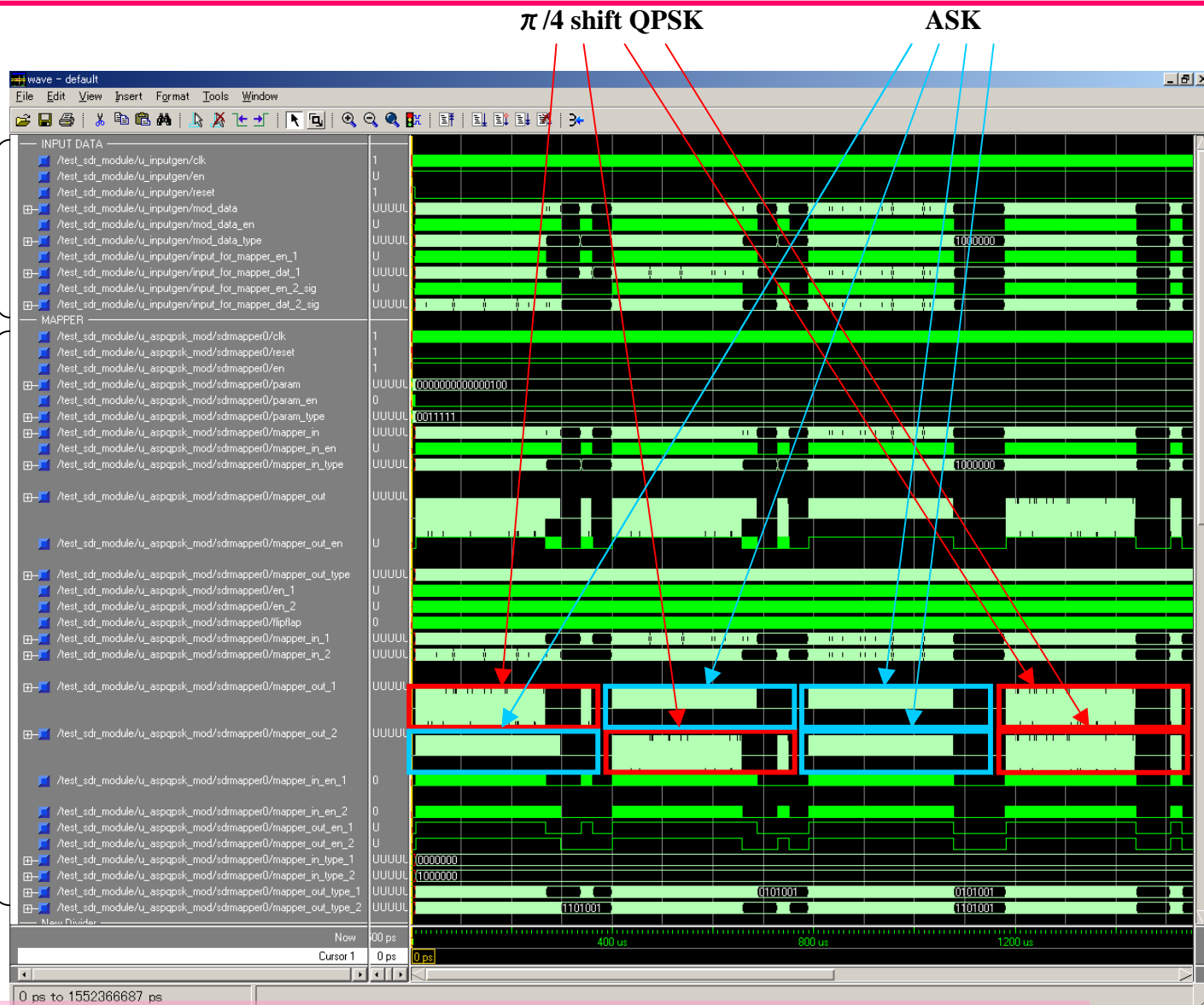
Each Demodulation Module for ASK and $\pi/4$ shift QPSK detect PR, UW pattern and output the output the demodulated data correctly

5-3. Simulation Results ~Multi-channel Modulation~

Input Signal
for ASK and QPSK
Modulation

Signals in
Mapper Module

Generated IQ Signal



IQ modulated signals are generated by any two combinations of modulation type(ASK and $\pi/4$ shift QPSK)

5-4. Simulation Results ~Multi-channel Demodulation~

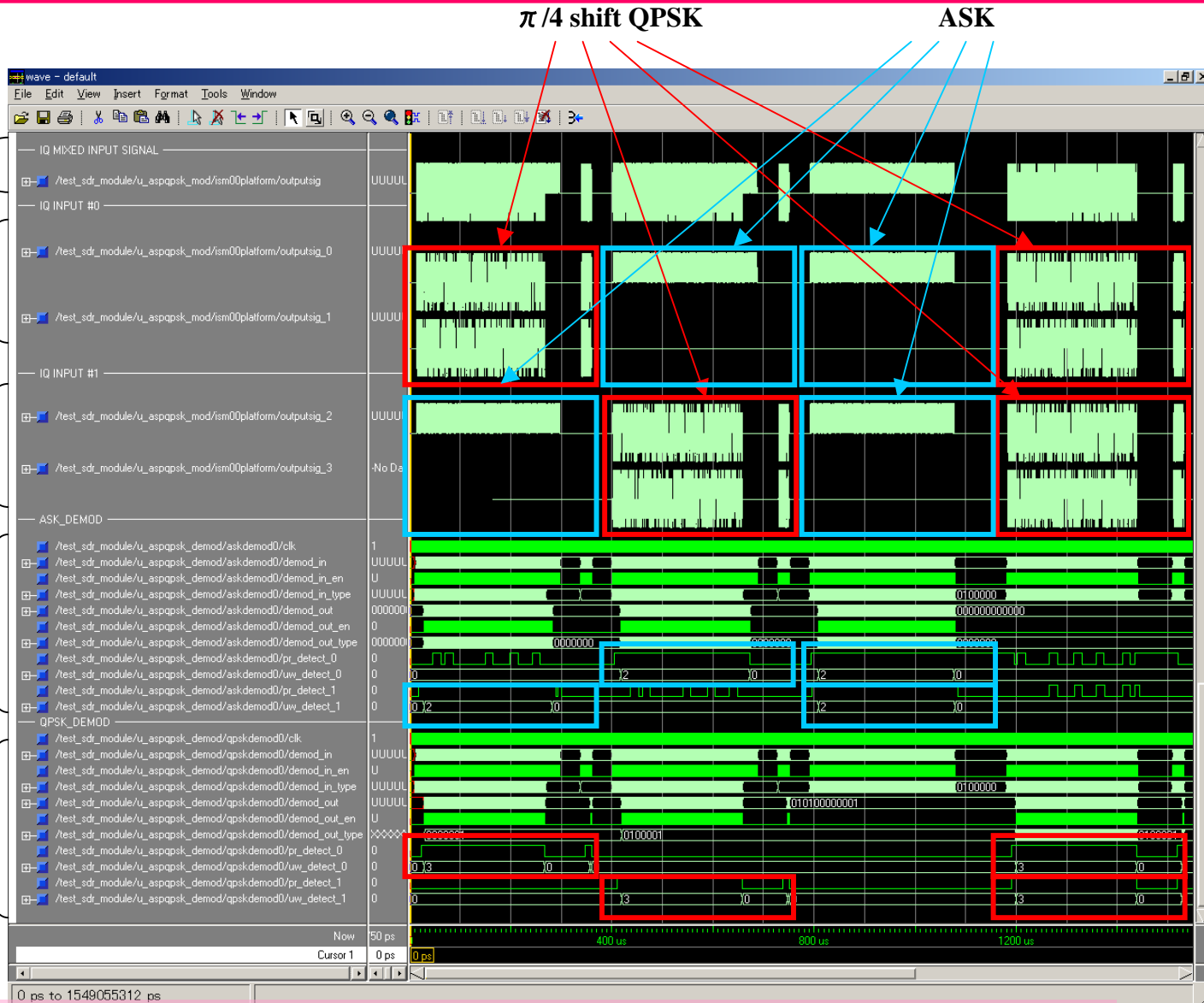
Input I,Q Signal (mixed)

Input I,Q Signal #1

Input I,Q Signal #2

Output signal from Demodulator for ASK

Output signal from Demodulator for QPSK



Each Demodulation Module for ASK and $\pi/4$ shift QPSK detect PR, UW pattern and output the output the demodulated data correctly.

- We explained
 - (1) **a packet routing-oriented signal processing platform(RPPP)**
with dynamic parameter reconfiguration for SDR
 - (2) the details of implementation
multi channel modem for DSRC system
based on our proposed signal processing platform
- We confirmed
The ability of multi-channel in parallel with efficient logic utilization
Logic count is totally improved by 20.18% compared with the fixed design